REMARKS

I. Claims 12 and 14 stand objected to for informalities. Claims 12 and 14 have been amended consistent with the Examiner's remarks to overcome the standing objections.

II. Claims 9-13 stand rejected under 35 USC 112, first paragraph, for the use of the term "laminated" in "laminated on" in line 4 of claim 9, and "preparing a laminated body" in line 3 of claim 9. This rejection is TRAVERSED as it is made without proper foundation. Nevertheless, the term "laminated" has been deleted from line 4 of claim 9, the term "laminated body" in line 3 of claim 9 remains.

It is well settled law that the claims of an application are to be interpreted in light of the specification and drawings. *Markman v. Westview Instruments, Inc.*, 116 S Ct 1384 (1996). It is also well settled law that any technical terms not interpreted in light of the specification and drawings are to be taken in their ordinary sense, as defined in a Technical Dictionary or other defining publication.

"Laminate" is defined in *McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition*, McGraw Hill Co., New York, 1974-2003) as: "a sheet of material made of several different bonded layers". The same Technical Dictionary defines "bond" as: "held together, adhered".

Moreover, it is clear from the specification to one of ordinary skill, that applicant's invention is a method of making a "wiring board", that is a "circuit board", specifically a "printed circuit board" of the type used in electronics and computers. This is evident from applicant's description of the prior art for which the present invention is an improvement. It is also evident from the prior art references cited against the pending claims. It is further obvious from the applicant's specification addressing his invention.

Applicant's specification at page 3, beginning at line 21 recites his invention as:

"... the present invention is to provide a process for manufacturing a wiring board capable of easily forming via recesses for filling with plating metal and of reducing the production cost of the wiring board.

... there is provided a process for manufacturing a wiring board, said process comprising the following steps of: making a resin plate having wiring pattern recesses and via through holes; coating all of the surfaces of the resin plate including inner walls of said wiring pattern recesses and via through holes with a metal film; applying an electro-plating using said metal film as a power-supply layer to fill a plated metal into said wiring pattern recesses and via through holes; and removing said metal film formed on said resin plate except for the inner walls of said wiring pattern recesses and via through holes, so that wiring pattern and vias are exposed on a surface the same as that of said resin plate.

The resin plate is formed by a press-forming process. Otherwise, the resin plate can be formed by an injection molding process.

The above mentioned process further comprises the following steps of: forming pads on one of surfaces of the wiring board to which external connecting terminals are to be attached.

The above mentioned process further comprises the following steps of: using said wiring board as a core substrate; and forming wiring patterns on the respective surface of the core substrate by means of resin layers to obtain a multi-layer wiring board.

According to another aspect of the present invention, there is provided a process for manufacturing a multi-layer wiring board, said process comprising:

a) manufacturing a core substrate comprising the steps of: making a resin plate having wiring pattern recesses and via through holes; coating all of the surfaces of the resin plate including inner walls of said wiring pattern recesses and via through holes with a metal film; applying an electro-plating using said metal film as a power supply layer to fill a plated metal into said wiring pattern recesses and via through holes; and removing said metal film formed on said resin plate except for the inner walls of said wiring pattern recesses and via through holes, so that wiring pattern and vias are exposed on a surface same as that of said resin plate; and

b) forming resin layers on respective surfaces of said core substrate so that said resin layers includes wiring pattern recesses and via through holes;

c) coating all of surfaces of said resin layers including inner walls of said wiring pattern recesses and via through holes with a metal film;

d) applying an electro-plating using said metal film as a power supply layer to fill a plated metal into said wiring pattern recesses and via through holes; and

(e) removing said metal film attached to said resin layer except for the inner walls of said wiring pattern recesses and via through holes, so that wiring pattern and vias are exposed on a surface same as that of said resin plate."

It is clear to one of ordinary skill in the art that the wiring board (printed circuit board) produced by applicant's novel process is a laminate (a lamination of various layers adhered together). This is true if applicant's process makes a board with one resin layer or with plural resin layers. With a single resin layer board, the other layer is the wiring pattern.

One of ordinary skill would first think of a wiring board as a planar wiring pattern adhered onto a planar resin board. Unless otherwise defined by an inventor, wiring boards are thought of as multi-layered planar laminations. Specifically, from applicant's specification, It is readily understood by one of ordinary skill, that applicant molds resin into a plate and then applies a metal layer to a surface of the resin plate. Applicant then converts the metal layer adhered to the surface of the resin plate into a wiring pattern. It is readily understood by one of ordinary skill that applicant's wiring board is a sheet-like structure and that a first layer of metal applied to the resin forms a lamination. It is further readily understood by one of ordinary skill that the successive plural layers formed by applicant's process provide further laminations.

Applicant's invention is an improved process of achieving the manufacture of a wiring board. Many wiring boards have a sheet (plate) resin core and a wiring pattern on a surface thereof, with via through holes. It is understood by one of ordinary skill in the art that a wiring board incorporates laminated construction.

35 USC 112, first paragraph, sets forth the minimum requirements for the quality and quantity of information that must be contained in a patent specification. The disclosure must have sufficient information to put the public in possession of the invention and to enable those skilled in the art to make and use the invention. MPEP 2162. To satisfy the written description requirement, a specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude the inventor has possession of the claimed invention. *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d at 1563, 19 USPQ at 1116 (Fed. Cir. 1991).

There is a strong presumption that an adequate written description of the claimed invention is present when the application is filed. The PTO has the initial burden of presenting evidence or reasons why persons skilled in the art would not recognize in the disclosure a description of the invention defined in the claims. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976).

The claimed invention, which is adequately described, or, which is conventional in the art or known to one of ordinary skill in the art cannot re rejected under 35 USC 112, first paragraph. MPEP 2163 (I)(A)

There is no *in haec verba* requirement for claim language with respect to the specification. Newly added claim limitations must be supported in the specification through "express", implicit", or "inherent" disclosure. *In re Oda* 443 F.2d 1200, 170 USPQ 268 (CCPA 1971); MPEP 2163 (I)(B). The fundamental factual inquiry is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date, applicant was in possession of the invention not claimed. *Vas-Cath, Inc. v. Mahurkar*, 935 F2d 1555, 19 USPQ2d 111 (Fed. Cir. 1991); MPEP 2163 (I)(B).

The examiner has the initial burden of presenting evidence or reasons why a person skilled in the art would not recognize that the written description provides support for the claims. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); MPEP 2163 (II)(A).

Where the examiner finds that the disclosure does not reasonably convey that the inventor had possession of the claimed subject matter of an amendment at the time of filing the application, the examiner has the initial burden of presenting evidence or reasoning to explain why persons skilled in the art would not recognize in the disclosure a description of the invention now defined by the claims. *In re Smith*, 458 F.2d 1389, 173 USPQ 679 (CCPA 1972); MPEP 2163 (II)(A).

In determining whether a specification complies with the disclosure requirement to support a claim, the examiner should make a determination of the field of the invention and the level of skill and knowledge In the art. Information which is well known in the art need not be described in detail in the specification. *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81 (Fed. Cir. 1986); MPEP 2163 (II) (A)(2).

An adequate written description may be shown by any description of sufficient, relevant, identifying characteristics so long as a person skilled in the art would recognize the inventor had possession of the claimed invention. This evaluation must be individually done for each application. *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 56 USPQ2d 1481 (Fed.Cir. 2000); *Pfaff v. Wells Electronics, Inc.* 55 US at 66, 119 Supreme Court at 311, 48 USPQ2d at 1646.

What is conventional or what is well known to one of ordinary skill in the art need not be disclosed in detail. *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81 (Fed. Cir. 1986); MPEP 2163 (II) (A)(2). The description need not be in *ipsis verbis* [i.e., "in the same words"] to be sufficient. *Martin v. Johnson*, 454 F.2d 746, 172 USPQ 391 (CCPA 1972).

Patents and printed publications in the art should be relied upon to determine whether an art is "mature" and what the "level of knowledge and skill" is in the art. In most technologies which are mature, a 35 USC 112 disclosure issue should not be raised. *In re Hayes Microcomputer Products, Inc. Patent Litigation*, 982 F.2d 1527, 25 USPQ2d 1241 (Fed. Cir. 1992); MPEP 2163 (II)(A)(3)(a)(i).

The description will be presumed to be adequate unless or until sufficient evidence or reasoning is presented by the examiner to rebut that presumption. *In re Marzocchi*, 439 F.2d 220, 169 USPQ 367 (CCPA 1971). The examiner, therefore, must present a reasonable basis for challenging the adequacy of a written description; and has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined in the claims. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); MPEP 2163 (III)(A). In rejecting a claim, the examiner must set forth express findings of fact regarding the above analysis which support the lack of written description conclusion. The examiner must establish a prima facie case by supporting the reasons why a person skilled in the art at the time the application was filed would not have

recognized that the inventor was in possession of the invention as claimed in view of the disclosure in the application. *In re Rasmussen*, 650 F.2d 1211, 211 USPQ 323 (CCPA 1981); MPEP 2163 (III)(A). Moreover, when appropriate, the examiner should suggest amendments to the claims which can be supported by the application's written description. MPEP 2163(III)(A).

The "standard" to be used is that an applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the application, and that the invention, in that context, is whatever is now claimed. The test for sufficiency of support is whether the disclosure "reasonably conveys" to the artisan that the inventor had possession at that time of the later claimed subject matter, i.e., that the specification conveys with reasonable clarity to those skilled in the art. Ralsont Purina Co. v. Far-Mar-Co., Inc. 772 F.2d 1570, 227 USPQ 177 (Fed. Cir. 1985); In re Kaslo, 707 F.2d 1366, 217 USPQ 1089 (Fed. Cir. 1983); MPEP 2163.02

Clearly, applicant's specification has adequately conveyed to one skilled in the art that the wiring board, made by his process, is layered and that the layers are adhered to one another (i.e., a laminate structure). This is true, whether applicant makes a single resin layer with a wiring pattern layer, or plural resin layers, each with a respective wiring pattern layer.

It is clear that the Examiner has not his burden of a *prima facie* showing. It is further clear that the level of skill in this art is such, as exhibited by the Examiner's reference, Tokuda (US 5,870,289), for example, that one of ordinary skill knows that a wiring board can be a laminate structure. The standing 35 USC 112, first paragraph, rejections of claims 9 - 13 cannot be sustained and must now be withdrawn.

III. Claims 6-14 stand rejected under 35 USC 112, second paragraphs, as being indefinite. In this regard the Examiner has questioned in claim 6, line 13 in the use of the term "wiring pattern", referring to claim 6, line 12. Further at claim 6, line 13 the Examiner has questioned

the terms "wiring pattern and vias"; and at lines 23-24 has question the terms "wiring pattern" and "wiring pattern and vias".

The Examiner has raised identical questions regarding identical type terms in claims 9, 12 and 14.

The language of claims 6-14 is reflected throughout the specification, including the summary of the invention reproduced in part hereIn above. The standing 35 USC 112, second paragraph, rejection of claims 6-14 is TRAVERSED.

It is apparent that the Examiner has miss-read applicant's disclosure in connection with the offered drawings. It is further apparent that the Examiner has miss-read the differences between the present invention and the prior art.

IV. Applicant's invention:

Applicant has invented a simple, cost effective and unobvious method for making a wiring board (printed circuit board). Applicant's process provides a wiring board that is made from a resin core sheet with via through-holes and a wiring pattern on one side thereof. Applicant repeats this method for making multi-layered boards. At page 3, lines 20-24 of the specification applicant expressly recites that an *object of his invention is to provide a process of manufacturing a wiring board with reduced cost*. The reason applicant's process reduces cost is that he reduces the number of process steps to make the wiring pattern and conductive vias, in that he has invented process steps not disclosed nor shown in the prior art for making a wiring pattern and conductive vias on a resin substrate (resin plate). Applicant's process steps are easier than those practiced in the prior art.

Applicant is not claiming the "structure" of a wiring board, but his unique and unobvious method for making the structure of a wiring board. Those of ordinary skill in this art know that a wiring board can be made by other methods. In fact, applicant's disclosure discusses prior art.

As it happens, applicant's unique method produces a unique wiring board feature, which is a product-by-process, but applicant has chosen not to claim that product by process.

With prior art wiring boards the wiring pattern (a metal film pattern) is adhered to the surface of the resin core sheet and therefore sits above the surface of the resin. The wiring boards produced by applicant's process have the wiring pattern positioned in a recess in the resin core sheet, which recess is the pattern of the desired wiring pattern.

In the prior art, a wiring board manufacturer generally starts with a flat resin sheet and drills vias through the sheet. One of ordinary skill in the art knows that vias are used to electrically connect the wiring pattern on one side of the board with the other side of the board. In the instance of multi-layered boards, the vias interconnect selected layers.

Applicant's unique and unobvious process first involves the molding by applicant of the resin sheet/ plate. However, applicant as part of his resin molding process, press forms molds the desired wiring pattern into one side of the resin sheet / plate by creating a wiring pattern shaped recession(s) in that side (face) of the resin sheet/ plate. This is plainly understood from a reading of the text of the specification. Moreover, at the same time, i.e., in the same press forming operation applicant makes the via through-holes in (through) the resin sheet/ plate. This is a one-step press molding operation.

Thereafter, applicant coats the entire molded resin plate, including all wiring pattern recessions (recesses) molded into the surface of resin plate and holes with a metal film. Then applicant applies an electro-plating to the entire molded resin plate using the previously applied metal film as a power-supply layer. The electro-plated metal coats every part of the resin sheet and fills both the formed wiring pattern recessions the vias (holes).

It is understood by one of ordinary skill that a wiring pattern recession is a recession in the surface (face) of the resin plate in the shape of the desired wiring pattern. It does not

become a wiring pattern until the recession is filled with plated metal and the excess is cleaned away.

It is understood by one of ordinary skill that the vias are selectively positioned through the resin plate/ sheet (core) to make connection with a selected portion of the eventual wiring pattern. It is also understood by one of ordinary skill that the wiring pattern shape or shapes is(are) designed for the particular electronic circuit for which the wiring board was designed.

Applicant then removes the plated metal from the surface of the resin plate by polishing. It is understood by one of ordinary skill that this polishing stops when gets down to the surface of the resin. Applicant's process produces a wiring board where the surface of the vias and the surface of the wiring patterns are at the same level as the surface of the resin plate. (See page 7, lines 8-12).

Applicant's unique and unobvious process produces a unique product where the wiring pattern film is imbedded in the surface (face) of the resin plate. Moreover, applicant has invented a simple process for providing this product by process.

The Examiner may have miss-read claims 6 - 14 because of the grammar. Therefore, claims 6, 9, and 14 are being amended herein above to recite better grammar, only. No new scope, and no new limitations have been added. However, applicant asserts that the claims 6, 9 and 14 as previously examined were clear, distinct, and definite to one of ordinary skill, who would have read applicant's specification in full.

The Examiner is reminded that an applicant is permitted to be his own lexicographer and that the meaning of his words are to be interpreted in light of his disclosure.

It is well settled law that the claims of an application are to be interpreted in light of the specification and drawings. *Markman v. Westview Instruments, Inc.*, 116 S Ct 1384 (1996). It is also well settled law that any technical terms not interpreted in light of the specification and

drawings are to be taken in their ordinary sense, as defined in a Technical Dictionary or other defining publication.

For all of these reasons the standing 35 USC 112, second paragraph, rejection of claims 6-11 and 13-14 cannot be sustained and must now be withdrawn.

V. Claim 12 stands rejected under 35 USC 112, second paragraph, for the allegedly confusing nature of element (a). To one at the level of those skilled in this art, the language of claim 12 is clear, and definite. Claim 12 recites that applicant is making successive layers for a multi-layered board, having first made a first layer by the steps of claim 9. It is clear that claim 9 as examined required the steps of claim 9 to be conducted as element (a) of claim 12. An equivalent manner of reciting this is now presented in amended claim 12 presented herein above. The Examiner should now withdrawn the § 112 rejection of claim 12.

VI. Claims 1-3, and 14 stand rejected under 35 USC 103(a) as obvious in view of Odaira et al. (US 5,333,379). Applicant asserts that the Examiner has miss-read this reference and therefore, this rejection is TRAVERSED.

Claim 4, stands rejected under 35 USC 103(a) as obvious in view of Odaira when read with Tokuda et al. (US 5,870,289). Applicant asserts that the Examiner has miss-read these references and therefore this rejection is TRAVERSED.

Claim 5 stands rejected under 35 USC 103(a) as obvious in view of Odaira when read with Koyama (US 6,254,758). Applicant asserts that the Examiner has miss-read these references and therefore this rejection is TRAVERSED.

Claims 6-8 stand rejected under 35 USC 103(a) as obvious in view of Odaira when read with Koyama. This rejection is TRAVERSED.

Claims 9-13 stand rejected under 35 USC 103(a) as obvious in view of Odaira when read with Koyama. This rejection is TRAVERSED.

VII. Law on showing obviousness:

The Examiner is required to set forth in his Office Action in support of a 35 USC 103 rejection the following: (A) the relevant teachings of the prior art relied upon, including making reference to the relevant column of page number(s) and the line number(s) where appropriate; (B) the difference or differences in the claim over the applied reference(s); (C) the proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter; and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification. See MPEP 706.02(j).

The Examiner has failed to adequately provide all four phases of this information. The MPEP is quite clear that all four phases (items (A) through (D)) must be made. The Examiner failed to address why one of ordinary skill in the art would at the time of the invention have been motivated to make the proposed modification. In failing to make the analysis phase (D) applicant believes the Examiner has misunderstood the structure and operation of the prior art and miss-read what the prior art states. Applicant's technical support will follow below.

In order to establish a *prima facie* case of obviousness the following three basic criteria must be met: 1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to combine the specific reference(s) teachings; 2) there must be a reasonable expectation of success in combining the specific reference(s) teachings; and 3) the prior reference (or references when combined) must teach or suggest all of the claim limitations. See MPEP 706.02. The teachings or "suggestion to combine" and the "reasonable expectation of success" must both be found in the prior art and not based upon the applicant's disclosure. *In re Vaeck*, 947 F2d 488, 20

USPQ2d 1438 (Fed Cir 1991). The initial burden is on the Examiner to provide support for a *prima facie* case. *Ex parte Clapp*, 277 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985).

VIII. Engineering analysis:

Odaira teaches a method of producing a three-dimensional wiring board. Odaira's process is as follows:

1) providing a two piece mold with a conductor circuit (wiring pattern) having small projections formed by electro-plating on the inner surface of each mold piece;

2) bringing the two pieces of the mold together in a pressure contact so that the conductor circuits on each mold piece inner surface are in contact with one another and held thereto by the interlocking of the projections;

3) filling the mold with resin so that the conductor circuits are "reversely" secured to the molded product to complete the production of the three-dimensional wiring board. (abstract, and col. 3, lines 23-47, and lines 66-68) It is the plastic deformation of the projecting tips that causes the two wiring patterns to interlock and be held in electric contact. (Col. 4, lines 3-12)

After these steps, Odaira removes filled resin from the molded product by dissolving this resin after the molded product having the conductor circuits reversely secured thereto is removed from the molding die and a number of electronic components are assembled on the molded product. (Col. 3, lines 47-53)

Odaira's process has no relation to the present invention whatsoever. The Examiner has also miss-read Odaira's Figs. 5-7 that show the Odaira product.

Furthermore, Odaira deposits his wiring pattern on his mold surfaces by standard resist layers, irradiation, insulating film and plating steps. (Col 5, lines 23-50). In his molding process, Odaira transfers his wiring patterns from his mold surfaces to his injected resin. These process steps have no relation to the present invention whatsoever.

Moreover, as Odaira has made contact between his wiring patterns with the projecting tips which deform to interlock two wiring patterns, Odaira has no need for vias. While Odaira does introduce an insulating outer resin 6, the purpose and use of this resin layer 6 is merely to encapsulate his electronic component 8 after it is mounted on his three-dimensional board. This additional process step has no relation to the present invention.

Additionally, Odaira clearly shows his wiring pattern, Figs. 5-7, to be at a different surface (level) than his resin. This likewise departs from the present invention.

Tokuda shows a flip-chip connection for a wiring showing a through-hole electrical connection, or via. Tokuda does not address the process steps for manufacturing his device, nor are the process steps of manufacture evident from the device itself. While Tokuda shows connecting pads 11 at the same surface (level) as the face of his adhesive film 30, the Tokuda connecting pads 11 and the through-hold connections 40 extend beyond the surface level of his resin substrate 20.

Like Odaira, Tokuda does not disclose nor suggest any process steps which would anticipate or obviate applicants claimed process. Moreover, there is no suggestion in the prior art of how or for what purpose Odaira and Tokuda could be combined. Nor is there a suggestion that such a combination might meet with success.

Koyama shows a method of forming a conductor pattern on a wiring board. This method includes the steps of:

1) forming an electroless copper (metal) plated layer on the surface of an insulating layer;

2) forming and patterning a layer of resist on the electroless copper layer;

3) exposing the layer of plated resist (in a pattern);

4) forming an elecrolytic copper plated layer on the electroless copper plated layer which had been exposed;

5) removing the layer of plated resist for exposing the elecroless copper except for a portion in which the electrolytic copper plated layer is formed; and

6) removing the exposed electoless coper plated layer by etching.

The Koyama process is a variation of the prior art photo process discussed by applicant as being the "damascene" method. Koyama utilizes a layer of photoresist, exposes a pattern and removes the portion exposed to leave a copper (metal) film in his desired pattern.

The Koyama process is not compatible with applicant's invention. Moreover, the Koyama adds no steps to the Odaira method which obviate applicant's invention. In fact, the Koyama steps have no meaning to the Odaira process and one of ordinary skill would not look to modify the Odaira process with any of the Koyama process steps. There would be no incentive to do so. There would be no anticipation of any success in making such a combination. Lastly, any combination would not yield a process which would anticipate or obviate applicant's process steps.

IX. Conclusion:

The Examiner has not met his burden of presenting a *prima facie* case under 35 USC 103(a).

Applicant has claimed a series of process steps to be preformed in a certain sequence. To obviate applicant's claimed process, the prior art must not only teach each of the exact process steps, which it clearly does not, but also must obviate the order (sequence) of the process steps of the present invention, which it also clearly does not.

It is urged that the application be re-examined and passed to issue with the claims as amended herein above. The Examiner is invited to telephone applicant's attorneys to resolve any remaining issues.

Respectfully submitted,

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